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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/069,054	04/28/1998	KING W. CHAN	ACT-233	2978

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Kenneth D' Alessandro
Sierra Patent Group, Ltd.
P.O. Box 6149
Stateline, NV 89449

EXAMINER	
GARBOWSKI, LEIGH M	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/069,054	CHAN ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-23 and 27-39* is/are rejected.

7)☒ Claim(s) *4-6 and 24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

The drawings are objected to because the interface buffers depicted in figure 11 should be designated by the number --26-- [see page 15, line 5]. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 7-16, 20-23, 27-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Beal et al. [U.S. Patent #6,150,837]

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1, an interface architecture in an IC comprising: an FPGA portion of said IC having logic blocks for implementing logic functions and interconnect conductors for programmably connecting said logic blocks [column 4, lines 35-45]; an ASIC portion of said IC having mask programmed logic circuits and mask programmed interconnect conductors between said logic circuits [column 4, lines 46-59]; and mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion [column 3, lines 39-40; column 5, lines 5-10]. As per claim 2, wherein interconnect conductors in said FPGA portion include local routing resources [an FPGA by definition]. As per claim 3, further including interface buffers disposed in series with said dedicated interface tracks between said FPGA portion and said ASIC portion [column 6, lines 5-10]. As per claim 7, further including an FPGA-ASIC routing channel arranged between said dedicated interface tracks and said ASIC portion [figure 4]. As per claims 8, 9, wherein said FPGA-ASIC routing channel is mask-programmable, field-programmable [column 10, lines 1-5, 66-67; column 11, lines 13-14]. As per claim 10, further including JTAG buffers arranged between said dedicated interface tracks and said ASIC portion [column 6, lines 5-10, 45-50]. As per claims 11, 12, 13,14, 15, 16, further including a plurality of I/O modules arranged on the perimeter of the IC, wherein one or more of said I/O modules are connected to said FPGA-ASIC routing channel, wherein one ore more of said I/O modules are connected to said ASIC portion, wherein said ASIC portion is adjacent to one side of said FPGA portion [figure 4]. As per claim 20, wherein said FPGA portion has a hierarchical design including a plurality of levels, each of said levels containing local routing resources and a plurality of blocks, each of said blocks including

either a module or another of said levels [this is by definition a FPGA, column 1, lines 6-7].

As per claim 21, an interface architecture in an IC comprising: an FPGA portion of said IC having a plurality of levels, each of said levels containing local routing resources and a plurality of blocks, each of said blocks including either a module or another of said levels [this is by definition an FPGA, column 1, lines 6-7; column 4, lines 35-45]; an ASIC portion of said IC having mask programmed interconnect conductors between said logic portions of said ASIC portion [column 4, lines 46-59]; mask programmed dedicated interface tracks connected between said modules or blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion [column 3, lines 39-40; column 5, lines 5-10]. As per claim 22, wherein each of said blocks in said FPGA portion contains local routing resources [an FPGA by definition]. As per claim 23, further including interface buffers arranged between said dedicated interface tracks and said ASIC portion [column 6, lines 5-10]. As per claim 27, further including an FPGA-ASIC routing channel arranged between said dedicated interface tracks and said ASIC portion [figure 4]. As per claims 28, 29, wherein said FPGA-ASIC routing channel is mask-programmable, field-programmable [column 10, lines 1-5, 66-67; column 11, lines 13-14]. As per claim 30, further including JTAG buffers arranged between said dedicated interface tracks and said ASIC portion [column 6, lines 5-10, 45-50]. As per claims 31, 32, 33, 34, 35, 36, further including a plurality of I/O modules arranged on the perimeter of the IC, wherein one or more of said I/O modules are connected to said FPGA-ASIC routing channel, wherein one ore more of said I/O modules are connected to said ASIC portion, wherein said ASIC portion is adjacent to one side of said FPGA portion [figure 4].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17-19, 37-39 are rejected under 35 U.S.C. 103(a) as being obvious over Beal et al.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Beal et al. disclose the limitations from which these claims depend, however, the reference does not explicitly teach the exact configuration relating to the placing of the ASIC portion with respect to the FPGA portion with respect to the present claims. Yet, Beal et al. disclose at least one side of the ASIC adjacent to the FPGA as shown above. Furthermore, Applicants' admitted prior art (AAPA) discloses these present limitations: Pursuant to claim 17 wherein said ASIC portion is adjacent to two sides of said FPGA portion: AAPA, Fig. 1C, 1D; Pursuant to claim 18 wherein said ASIC portion is adjacent to three sides of said FPGA portion: AAPA, Fig. 1C, 1D (including the side between the I/O and the FPGA and ASIC); Pursuant to claim 19 wherein said ASIC portion is adjacent to four sides of said FPGA portion: AAPA, Fig. 1E, 1F. Therefore, it would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to exercise their design prerogative and modify the design architecture of Beal et al.,

and to rely on, consider, and incorporate what is already well known prior art in determining further improvements, to facilitate a routing or timing objective by making the ASIC portion adjacent to two, three or four sides of the FPGA portion.

Allowable Subject Matter

Claims 4-6 and 24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not disclose, teach, or suggest the particular features that each of the interface buffers include.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Joly et al. [U.S. Patent #6,334,207 B1] disclose an interface between an FPGA and an ASIC [figure 3, element 308].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER